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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,843	10/08/2004	Kevin Lin	61994.00018	5842

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EXAMINER	
ELAND, SHAWN	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,843	LIN, KEVIN	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Formal Matters

This Office action is in response to the Applicant's response filed on January 15, 2007.

Status of Claims

Claims 1 – 20 are pending in the Application.

Claims 5 – 6, 12, & 20 have been amended.

There are no cancelled claims.

There are no new claims.

Claims 1 – 20 are rejected.

Response to Arguments

Claim 1 – 11, & 17 – 20 remain rejected under the same grounds as the previous Office action – that is under Chowdhary (US 6,675,278) in view of Ryan (US 5,748,551).

Applicant's arguments filed January 15, 2007 have been fully considered but they are not persuasive. The Examiner respectfully disagrees with Applicant's argument that the modification made would "defeat Chowdhary's purpose" since Ryan states that the different memory banks appear to be one contiguous piece of memory (see column 6, lines 15 – 19). Appearing as a single memory space is irrelevant. Chowdhary will optimize the "contiguous" memory space, but it is Ryan that writes to one bank while the other is pre-charging. Ryan certainly suggests that the adjacent logical blocks can, in

fact, be stored physically at different banks of memory (see column 6, lines 22 – 28). In addition, Ryan also states that the concept of storing logically adjacent blocks of data across different physical memory banks was well known in the art (see column 3, lines 1 – 10). Examiner firmly, but respectfully, believes there is plenty of prior art and that there is nothing novel and non-obvious as claimed in Applicant's invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 11, & 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over under ***Chowdhary*** (US 6,675,278) in view of ***Ryan*** (US 5,748,551).

In regard to claim 1, Chowdhary teaches generating a block index for a block of data (see element 3 in figures 1 – 5; see column 2, lines 36 – 40); mapping the block index to a physical address of a memory (see column 2, lines 41 – 45); storing the block of data into the memory at the physical address (see column 2, lines 41 – 45).

Chowdhary does not teach mapping to physical memory based on the block index and a number N, wherein N is bank number of the memory; and looping to the generating step, wherein the mapping step makes each one of the block indexes map in turns to one physical address located at different banks, and result in any logical adjacent block of data be stored physically at different banks of the memory.

Ryan teaches mapping to physical memory based on the block index and a number N, wherein N is bank number of the memory and looping to the generating step, wherein the mapping step makes each one of the block indexes map in turns to one physical address located at different banks, and result in any logical adjacent block of data be stored physically at different banks of the memory (see column 3, lines 66 – 67 through column 4, lines 1 – 13). (It is inherent that Ryan's mapping also involves a number N as the invention needs to know how to divide the data into subarrays internally and yet appear as one contiguous memory externally. See also column 6, lines 15 – 19.) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory device to Chowdhary's invention as it would reduce useless wait cycles.

In regard to claim 17, Chowdhary teaches generating a plurality of block indexes for a plurality of blocks of data (see element 3 in figures 1 – 5; see column 2, lines 36 – 40); mapping the block indexes sequentially to a plurality of physical address of a memory (see column 2, lines 41 – 45); and storing the block of data into the memory at the physical address (see column 2, lines 41 – 45).

Chowdhary does not teach mapping to physical memory based on the block indexes and a number N, wherein N is bank number of the memory, wherein the mapping step makes each one of the block indexes map in turns to one physical address located at different banks, and result in any logical adjacent block of data be stored physically at different banks of the memory.

Ryan teaches mapping to physical memory based on the block indexes and a number N, wherein N is bank number of the memory, wherein the mapping step makes each one of the block indexes map in turns to one physical address located at different banks, and result in any logical adjacent block of data be stored physically at different banks of the memory (see column 3, lines 66 – 67 through column 4, lines 1 – 13). (It is inherent that Ryan's mapping also involves a number N as the invention needs to know how to divide the data into subarrays internally and yet appear as one contiguous memory externally. See also column 6, lines 15 – 19.) It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory device to Chowdhary's invention as it would reduce useless wait cycles..

In regard to claim 6, Chowdhary teaches retrieving a block of data from a source media (see column 3, lines 4 – 8); assigning a block index for the block of data (see element 3 in figures 1 – 5; see column 2, lines 41 – 45); storing the block of data in the memory at a physical address (see column 2, lines 41 – 45); and repeating form the retrieving step (this is inherent as the system is designed to handle multiple blocks),

Chowdhary does not teach dividing value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is bank number of the memory; calculating the physical address based on Q and R; and wherein the calculating step makes the block index interleaved mapping to the physical address located at different banks and any two logically successive blocks of data be stored physically at different banks of the memory.

Ryan teaches dividing value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is bank number of the memory (see column 3, lines 66 – 67 through column 4, lines 1 – 13; Ryan's invention divides mapping the physical memory between N number of banks, leaving Q & R, in order to define the subarrays within the system.); calculating the physical address based on Q and R (this is inherent to defining the subarrays; see column 6, lines 15 – 19); and wherein the calculating step makes the block index interleaved mapping to the physical address located at different banks and any two logically successive blocks of data be stored physically at different banks of the memory (see column 3, lines 66 – 67 through column 4, lines 1 – 13). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory device to Chowdhary's invention as it would reduce wait cycles.

In regards to claims 2 – 3, 7 – 8, & 18 – 19, Chowdhary does not teach wherein the memory supports pipelining access or is an SDRAM. Ryan, however, does (see column 1, lines 37 – 39; see Abstract, lines 17 – 21). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add these elements to Chowdhary's invention in order to better optimize RAM access.

For claims 4 – 5, 9 – 10, & 20 Chowdhary doesn't teach dividing the block index by N to obtain a quotient Q and a remainder R; and calculating the physical address based on Q and R, wherein the physical address=Q*block_size+R*bank_size wherein bank_size equals the memory size divided by N, and block_size equals the size of which the system is in need to process one sector from an optical disc.

Ryan teaches dividing the block index by N to obtain a quotient Q and a remainder R (see column 3, lines 66 – 67 through column 4, lines 1 – 13); and calculating the physical address based on Q and R (this is inherent to defining the subarrays; see column 6, lines 15 – 19), wherein the physical address=Q*block_size+R*bank_size (Dividing the memory into N equal-sized banks and writing to adjacent blocks in equal time intervals and block sizes as specified in this invention in column 3, lines 66 – 67 through column 4, lines 1 – 13 does just this.) wherein bank_size equals the memory size divided by N (This is inherent when memory is sum of all equally-sized memory banks), and block_size equals the size of which the system is in need to process one sector from the optical disc (see column 13, lines 61 – 64). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory system to Chowdhary's method of managing memory as it would expand his system by allowing for reading and writing to optical drives.

For claim 11, Chowdhary teaches reading the block of data according to the block index (see column 2, lines 41 – 45).

Chowdhary does not teach reading the block of data according to the reference function; and recording the block of data to a destination media, whereby the reading step makes each one of the block of data read at different banks in turns and result in time saving and reduces pre-charge overloads by reading in one bank and pre-charge in another bank accessed just before.

Ryan teaches reading the block of data according to the reference function (see column 6, lines 15 – 19); and recording the block of data to a destination media (see column 13, lines 61 – 64), whereby the reading step makes each one of the block of data read at different banks in turns and result in time saving and reduces pre-charge overloads by reading in one bank and pre-charge in another bank accessed just before (see column 8, lines 2 – 5). It would have been obvious to a person having ordinary skill in the art at the time the invention was made add Ryan's memory device to Chowdhary's invention as it would reduce useless wait cycles.

Claims 12 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over under ***Chowdhary*** (US 6,675,278) in view of ***Ryan*** (US 5,748,551) and ***Duncan*** (US 5,832,213).

In regards to claim 12, Chowdhary teaches; means for generating a block index for the block of data ***(see element 3 in figures 1 – 5; see column 2, lines 41 – 45)***; means for dividing value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is bank number of the memory ***(see column 3, lines 66 – 67 through column 4, lines 1 – 13)***; and means for calculating the physical address based on Q and R ***(see column 6, lines 15 – 19)***.

Chowdhary does not teach wherein the calculating means makes the block index interleaved mapping to the physical address located at different banks and any two logically successive blocks of data be stored physically at different banks of the memory. Ryan, however, does ***(see column 3, lines 66 – 67 through column 4, lines***

1 - 13). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory device to Chowdhary's invention as it would reduce wait cycles.

Chowdhary also does not teach means for retrieving a block of data from a disc, but Duncan does ***(see column 6, lines 2 – 6)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add this device for managing removable media in order to gain more control over the volume management interface.

Regarding claims 13 – 14, Chowdhary does not teach wherein the memory supports pipelining access or is an SDRAM. Ryan, however, does ***(see column 1, lines 37 – 39; see Abstract, lines 17 – 21)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add these elements to Chowdhary's invention in order to better optimize RAM access.

For claims 15 – 16, Chowdhary doesn't teach dividing the block index by N to obtain a quotient Q and a remainder R; and calculating the physical address based on Q and R, wherein the physical address=Q*block_size+R*bank_size wherein bank_size equals the memory size divided by N, and block_size equals the size of which the system is in need to process one sector from the optical disc.

Ryan teaches dividing the block index by N to obtain a quotient Q and a remainder R *(see column 3, lines 66 – 67 through column 4, lines 1 – 13)*; and calculating the physical address based on Q and R ***(this is inherent to defining the subarrays; see column 6, lines 15 – 19)***, wherein the physical

address=Q*block_size+R*bank_size ***(Dividing the memory into N equal-sized banks and writing to adjacent blocks in equal time intervals and block sizes as specified in this invention in column 3, lines 66 – 67 through column 4, lines 1 – 13 does just this.)*** wherein bank_size equals the memory size divided by N ***(This is inherent when memory is sum of all equally-sized memory banks)***, and block_size equals the size of which the system is in need to process one sector from the optical disc ***(see column 13, lines 61 – 64)***. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add Ryan's memory system to Chowdhary's method of managing memory as it would expand his system by allowing for reading and writing to optical drives.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner's Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SE

Shawn Eland
03/31/07

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
4-02-07